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Abstract of the Disclosure

A method is described for conveying payload timing information between a source and destination over an asynchronous network, such as an ATM network, wherein data is transmitted packets include header and payload fields. The packets are emitted at the source at a rate related to the payload timing information, which is recovered at the destination from the rate of arrival of the packets.

End-to-end Clock Recovery for ATM Networks

This invention relates to the field of telecommunications, and more particularly to a method and apparatus for conveying timing information in packet switched networks, such as ATM (Asynchronous Transfer Mode) networks.

In order to deliver real time interactive services, such as voice telephony, in ATM networks, timing information must be provided in conjunction with the payload information. This timing information is used for the synchronization of encoded payload at the user's decoder/encoder.

The existing telephone network is a synchronous Time Division Multiplexed (TDM) network. This digital network (PSTN -Public Switched Telephone Network) uses 8 kHz timing information for synchronization and delivery of real-time information with a constant delay between two end points, e.g., a telephone conversation.

A B-ISDN (Broadband Integrated Services Digital Network) network uses Asynchronous Transfer Mode (ATM) technology for transport and switching. To transport real-time information such as voice telephony between PSTN/PBXs synchronous networks and B-ISDN (ATM) asynchronous networks, some means must be provided to convey end-to-end timing information for the encoded information.

A known method for conveying timing information makes use of loop-timing. Loop-timing uses the physical layer of the interface to encode and transport 8 kHz timing information from the switch to the endstation. With this method the synchronization must be extended from the narrowband TDM PSTN or private PBX network to the ATM network. However,

most ATM premise equipment manufactured and sold today cannot deliver 8 kHz timing information using loop-timing. An object of the present invention is to overcome this disadvantage.

Accordingly the present invention provides a method of conveying payload timing information between a source and destination over an asynchronous network wherein data is transmitted packets include header and payload fields, comprising the steps of emitting said packets at the source at a rate related to the payload timing information; and recovering said timing information at the destination from the rate of arrival of said packets.

Preferably, said network is an ATM network, in which case said packets are ATM cells.

While the method in accordance with the invention will be described in connection with 3.1 kHz μ-Law or A-Law encoded 64 kbit/s PCM information, it is applicable to other data rates and other encoding schemes. This end-to-end clock recovery method described is transmission rate and ATM Adaptation Layer (AAL) independent. It can be used for any application and any AAL where delivery of end-to-end timing information is required, such as, telephony voice, H.320 video, encrypted data, etc.

For 64 kbit/s μ-Law or A-Law PCM encoded information, one octet of PCM encoded information is transmitted (64 kbit/s) every 125 µs. If a cell PDU (Payload Data Unit) size of 48 octets (AAL 0) is used, it would take 6 ms. For a cell PDU size of 47 octets (AAL 1) it would take 5.875 ms. It can be deduced that in a constant bit rate service, a 48 octet PDU size cell is received every 6 ms for the duration of the

connection. For a cell PDU size of 47 octets, it would be 5.875 ms. Therefore, the ATM source will emit ATM cells every 6 ms to the ATM network. For different data rates, e.g., 384 kbit/s it would be one cell per 1 ms for 48 octet PDU cell size.

For 64 kbit/s data rates;

one octet every 125 μs = 64 kbits/s

and ATM PDU cell size = 48 octets (AAL 0)

Therefore; ATM PDU size x data transmission rate = cell emission rate

48 x 125μs= 6 ms

For 384 kbit/s data rates, which is equivalent to 6 octets every 125 μs

48 x 125μs/6= 1 ms

Below is a table showing several different data rates and the calculated cell emission rate for cell PDU size of 48 octets (AAL 0).

Table 1: Cell Emission Rate for different data rates (AAL 0)

Number of Channels	Data Rate Kbit/s	Cell Size in Octets	Cell Emission Rate in msec.
1	64	48	6
2	128	48	3
3	192	48	2
4	256	48	1.5
5	320	48	1.2
6	384	48	1

8	512	48	0.75
10	640	48	0.6
12	768	48	0.5
15	960	48	0.4
16	1024	48	0.375
20	1280	48	0.3
24	1536	48	0.25
25	1600	48	0.24
30	1920	48	0.2
32	2048	48	0.1875
40	2560	48	0.15
48	3072	48	0.125
50	3200	48	0.12
60	3840	48	0.1
64	4096	48	0.09375
75	4800	48	0.08
80	5120	48	0.075
96	6144	48	0.0625
100	6400	48	0.06
120	7680	48	0.05
125	8000	48	0.048
128	8192	48	0.046875

For ATM PDU size of 47 octets (AAL 1) there is only one practical data rate: 64 kbit/s, since 47 is a primary number. Therefore the cell emission rate is;

47 x 125 μs = 5.875 ms

The invention also provides an arrangement for conveying payload timing information between a source and destination

over an asynchronous network wherein data is transmitted packets include header and payload fields, comprising a packet emitter at said source for emitting packets over a constant bit rate virtual connection through said network; clock means for controlling the rate of emission of said cells from said cell emitter with reference to the payload timing information to be conveyed; a cell receiver at the destination for receiving said cells from the network; and a payload clock recovering said timing information at the destination from the rate of arrival of incoming cells.

The invention will now be described in more detail, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 is a block diagram of a system in accordance with the invention;

Figure 2 shows an ATM cell header format (UNI);

Figure 3 shows cell flow in an ATM CBR connection;

Figure 4 is a block diagram of a clock control and filter circuit; and

Figure 5 is a timing diagram showing VCO tracking of received cell emission rate.

Referring to Figure 1, a source 1 is connected to a destination 5 via a virtual connection established through an ATM network in a conventional manner.

Source 1 includes a cell emitter 3 that emits ATM cells 4 over a constant bit rate, virtual connection at a rate that is related to payload clock 2, which references the timing information for the payload data of the ATM cells 4.

At the destination 5, the ATM cells 4 are received by cell receiver 6, which transfers the cells to read buffer 14. The rate of arrival of cells is timed by timer 10 and averaged by averaging circuit 11. Destination payload clock 12 generates payload clock signals referenced to the average rate of arrival of cells at cell receiver 6.

Thus, it will be seen that the cell emission rate of the virtual connection (VC) is used to convey the timing information for a constant bit rate (CBR) ATM connection between the source 1 and the destination 5. The timer 10 is also used to detect lost or severely delayed cells because the ATM network has a low probability that cells may be lost or delayed due to switch congestion or bit errors.

At the desination 5, the clock rate is adjusted to determine how quickly the received information will be read out from the receive buffer 14. The rate of reading information from the buffer must equal the rate of information being written into the buffer. If this relationship can be maintained, there will be no over-run or under-run of the receive buffer.

Each cell 4 that is transmitted from the cell emitter 3 has a five octet header. The header is used for routing of the cell in ATM switches. Figure 2 is a diagram of cell header format. The fifth octet of the header is called "Header Error Control" (HEC). It is used for detection/correction of bit errors in the ATM cell header. This HEC octet is used to convey the cell emission rate of the transmitter over the Virtual Connection (VC).

The properties of the ATM network are such that the network will introduce a cell delay variation (CDV) or jitter for

any CBR connection. Also, cells can be lost or severely delayed (greater than CDV of the VC) in the network. Therefore, the method must be able to convey timing information under the above conditions.

First it must be determined when an ATM cell is lost or severely delayed. This is accomplished by using the timer (Timer_A in Figure 3) that times the arrival interval between cells. The reception of a "Header Error Control" (HEC) octet in the VC that requires timing information to be conveyed is used to trigger Timer_A. Under normal conditions, a 48 octet PDU cell size will arrive every 6 ms. for 64 kbit/s service. The maximum CDV of the ATM network will be determined using signaling and added to the total delay. For this example a CDV of 2 ms maximum will be used. Therefore, Timer 10 is set to PDU cell segmentation delay plus the maximum CDV of the network connection; 6 ms + 2 ms = 8 ms.

The expiration of Timer_A indicates that a cell has not arrived for the virtual channel in question within the time allowed (8 ms), and therefore the cell is lost or severely delayed. A severely delayed cell is a cell that has a longer delay than what was negotiated by signaling at the beginning of the connection. For one or more cells that are lost or not delivered in time, one or more dummy cells containing silence information are to the payload for voice connections. This keeps the buffer at the right level (no underflow). Also the system keeps track of how many dummy cells were added.

Figure 3 shows cells being packaged and transmitted at fixed time intervals, every 6 ms. At the destination, it shows

that cells arriving at the receiver with some CDV (Cell Delay Variation). In this example, cell n+2 was lost in the ATM network. A dummy cell was added to maintain proper information flow from the buffer to the decoder. This locally generated dummy cell is of the same frequency and phase as the locally generated cell emission rate pulse. Therefore there is no VCO clock adjustment on the insertion of a dummy cell.

At the source, the cell emission clock is referenced to the information encoder (payload) clock 2. Therefore the transmitter's encoding clock can be recovered at destination by determining the rate of arrival of incoming cells. Any cell that is not delivered must be substituted with dummy silence cell so that the decoder will receives cell every 6 ms or an octet every 125 μs.

The ATM network delivers the payload (cells) with jitter (CDV) of 2 ms in this example. This cell reception jitter needs to be filtered. Figure 4 shows a simplified block diagram of Digital Frequency/Phase Detector which will determine if the receive payload clock 12 is running slow or fast. This detector compares the phases of the two clocks and decides if the frequency (f_x) of the VCO needs to be increased or decreased.

The circuit for extracting the clock signals from the incoming cells is shown in more detail in Figure 4. Digital frequency and phase detector 20 receives at its inputs the incoming cell arrival rate and the generated clock frequency f_x at the destination 5. The detector 20 generates respective down or up pulses connected through tri-statable buffers 21, 22 to integrator 23 whose output is connected to

voltage controlled oscillator 24 generating the recovered clock signal f_x. This signal f_x is the applied through divider 25 as the feedback signal to the second input of the detector 20.

Figure 5 is a timing diagram showing the two clock rates and how the digital frequency/phase detector generates pulses to the integrator 13 for adjustment of the frequency of VCO 14.

The purpose of the integrator 23 is to control the rate of change of output frequency the VCO 24. The integrator 23 can change the voltage threshold to the VCO 24. The rate of voltage change to the integrator 23 is programmed by resistor R1 and capacitor C1. The duration of the change is controlled by the width of "Up" or "Down" pulses output by the detector 20. If there is no pulse from the digital Frequency/Phase Detector, the integrator will produce a constant voltage level to the VCO 14, which will hold its frequency.

The described end-to-end clock recovery method can convey timing information over asynchronous ATM networks without the need of 8 kHz frame information being encoded into the physical interfaces. The described method works over current ATM networks and does not require any additional bandwidth or control information from the ATM network. The method is transparent to the ATM network.

THE EMBODIMENTS OF THE INVENTION IN WHICH AN EXCLUSIVE PROPERTY OR PRIVILEGE IS CLAIMED ARE DEFINED AS FOLLOWS:-

1. A method of conveying payload timing information between a source and destination over an asynchronous network wherein data is transmitted packets include header and payload fields, comprising the steps of:

emitting said packets at the source at a rate related to the payload timing information; and

recovering said timing information at the destination from the rate of arrival of said packets.

2. A method as claimed in claim 1, wherein said network is an ATM network and said packets are ATM cells.

3. A method as claimed in claim 2, further comprising the step of generating clock signals for the payload at the destination from said timing information.

4. A method as claimed in claim 3, wherein each cell has a header error control byte (HEC), and the rate of arrival of incoming cells is determined by detecting incoming HECS.

5. A method as claimed in claim 3, wherein rate of arrival and phase difference of incoming cells at the destination are used to adjust a clock generating said clock signals at the destination.

6. A method as claimed in claim 5, wherein the duration of the adjustment is controlled by the width of "Up" or "Down" pulses.

7. A method as claimed in claim 5, further comprising timing the arrival of HEC bytes, and ignoring bytes arriving outside predefined limits.

8. A method as claimed in claim 7, further comprising adding dummy cells to maintain proper information flow to the decoder when said bytes outside predefined limits are detected.

9. A method as claimed in claim 8, further comprising filtering out the cell delay variation for the connection.

10. A method as claimed in claim 9, further comprising using the recovered timing information to control the receive buffer read rate to prevent buffer over-run or under-run at the destination.

11. An arrangement for conveying payload timing information between a source and destination over an asynchronous network wherein data is transmitted packets include header and payload fields, comprising:

a packet emitter at said source for emitting packets over a constant bit rate virtual connection through said network;

clock means for controlling the rate of emission of said cells from said cell emitter with reference to the payload timing information to be conveyed;

a cell receiver at the destination for receiving said cells from the network;

and a payload clock recovering said timing information at the destination from the rate of arrival of incoming cells.

12. An arrangement as claimed in claim 11, wherein said network is an ATM network and said packets are ATM cells.

13. An arrangement as claimed in claim 3, wherein each cell has a header error control byte (HEC), and the rate of

arrival of incoming cells is determined by detecting incoming HECS.

14. An arrangement as claimed in claim 13, further comprising means for generating clock signals at the destination, and a rate of arrival and phase detector responsive to said incoming cells and said clock signals to control said clock signal generating means in a feedback arrangement.

15. An arrangement as claimed in claim 14, wherein said detector generates "Up" and "Down" pulses and the duration of a change signal applied to said clock signal generating means is determined by the width thereof.

16. An arrangement as claimed in claim 15, further comprising means for timing the arrival of HEC bytes and ignoring bytes arriving outside predefined limits.

17. An arrangement as claimed in claim 16, further comprising means for adding dummy cells to maintain proper information flow to the decoder when incoming bytes are ignored.

18. An arrangement as claimed in claim 17, further comprising means for filtering out the cell delay variation for the virtual connection.

19. An arrangement as claimed in claim 18, wherein said means for filtering out the cell delay variation for the virtual connection is an intgrator.

20. An arrangement as claimed in claim 18, wherein the recovered timing information is used to control the receive buffer read rate to prevent buffer over-run or under-run at the destination.

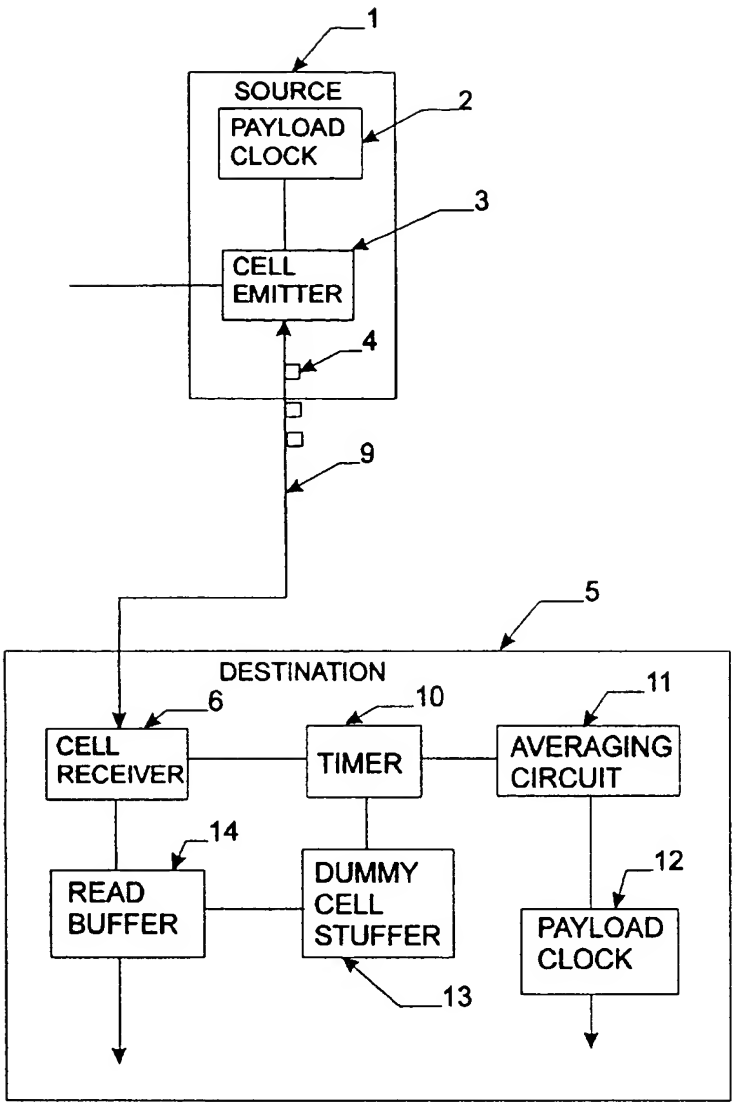
1
SOURCE
2
PAYLOAD CLOCK
3
CELL EMITTER
4
9
5
DESTINATION
6
10
11
CELL RECEIVER
TIMER
AVERAGING CIRCUIT
14
12
READ BUFFER
DUMMY CELL STUFFER
PAYLOAD CLOCK
13

Fig. 1

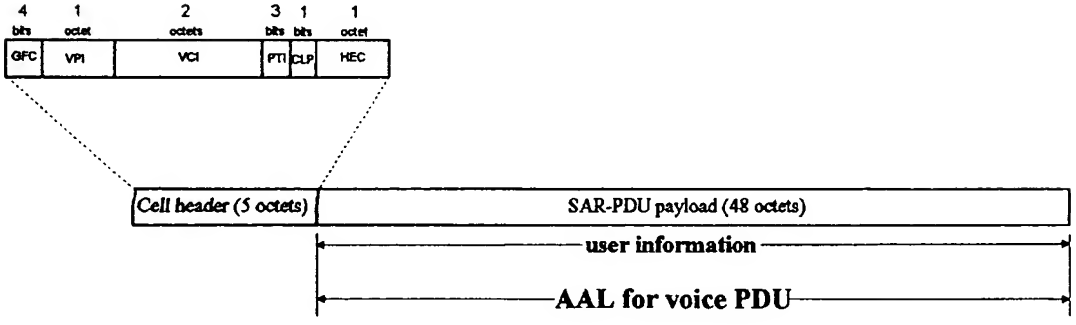
4 bits
1 octet
2 octets
3 bits
1 bits
1 octet
GFC
VPI
VCI
PTI
CLP
HEC
Cell header (5 octets)
SAR-PDU payload (48 octets)
user information
AAL for voice PDU

Fig. 2

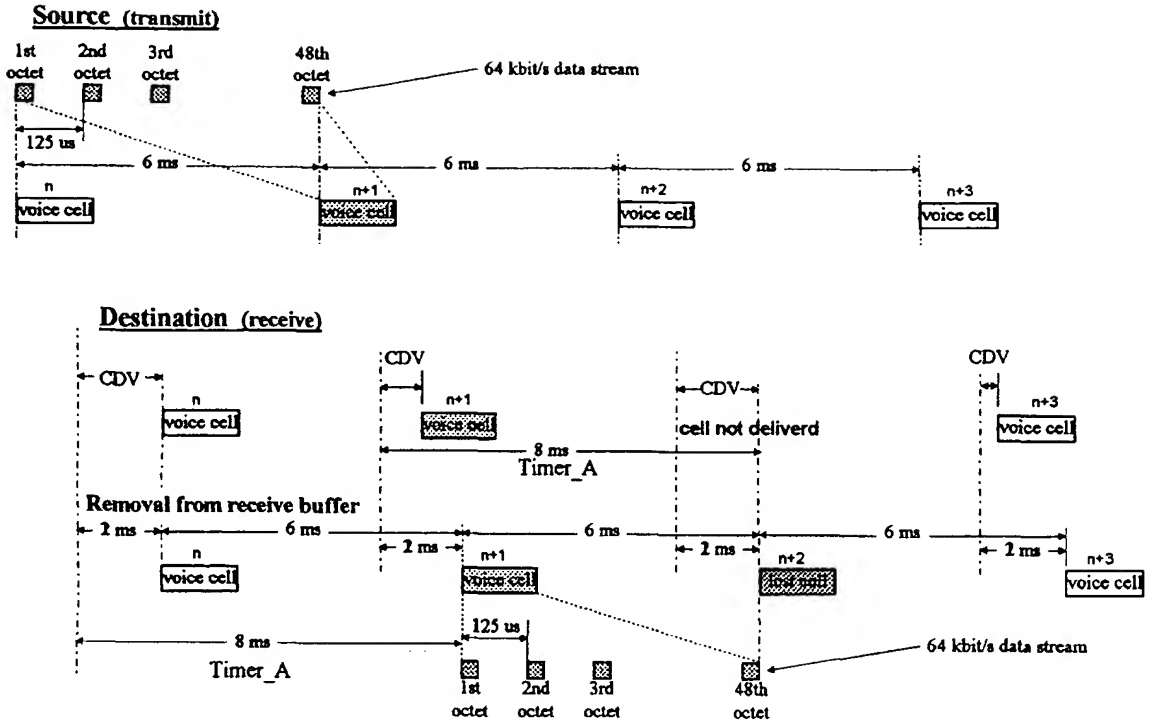
Source (transmit)
1st octet
2nd octet
3rd octet
48th octet
64 kbit/s data stream
125 us
6 ms
6 ms
6 ms
n
voice cell
n+1
voice cell
n+2
voice cell
n+3
voice cell
Destination (receive)
CDV
n
voice cell
CDV
n+1
voice cell
CDV
cell not deliverd
CDV
n+3
voice cell
8 ms
Timer_A
Removal from receive buffer
2 ms
6 ms
2 ms
6 ms
2 ms
6 ms
2 ms
n
voice cell
n+1
voice cell
n+2
n+3
voice cell
125 us
8 ms
Timer_A
64 kbit/s data stream
1st octet
2nd octet
3rd octet
48th octet

Fig. 3

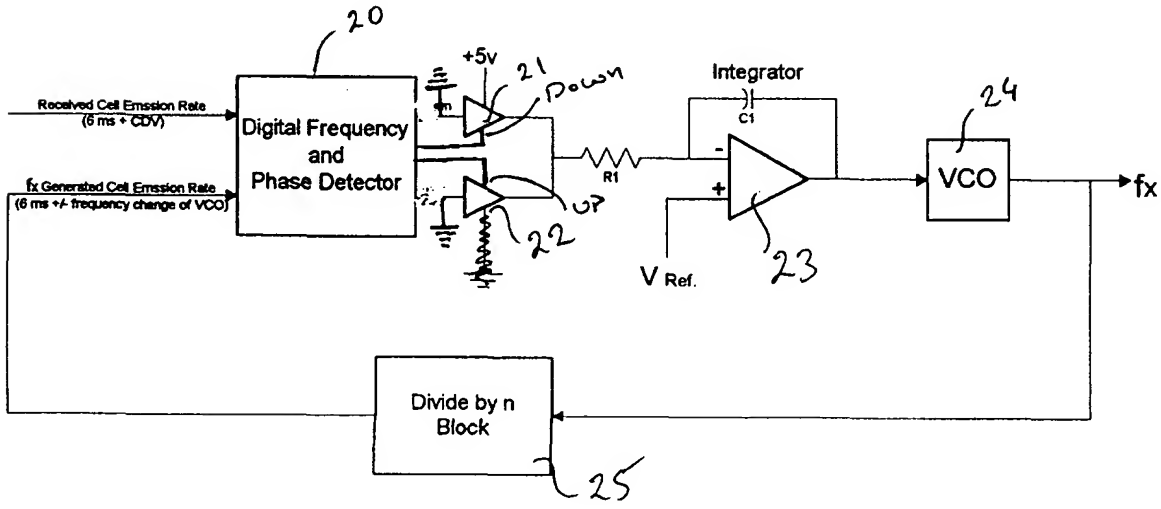
20
Received Cell Emission Rate
(6 ms + CDV)
fx Generated Cell Emission Rate
(6 ms +/- frequency change of VCO)
Digital Frequency
and
Phase Detector
+5v
21
Down
UP
22
R1
Integrator
C1
V Ref.
23
24
VCO
fx
Divide by n
Block
25

Fig. 4

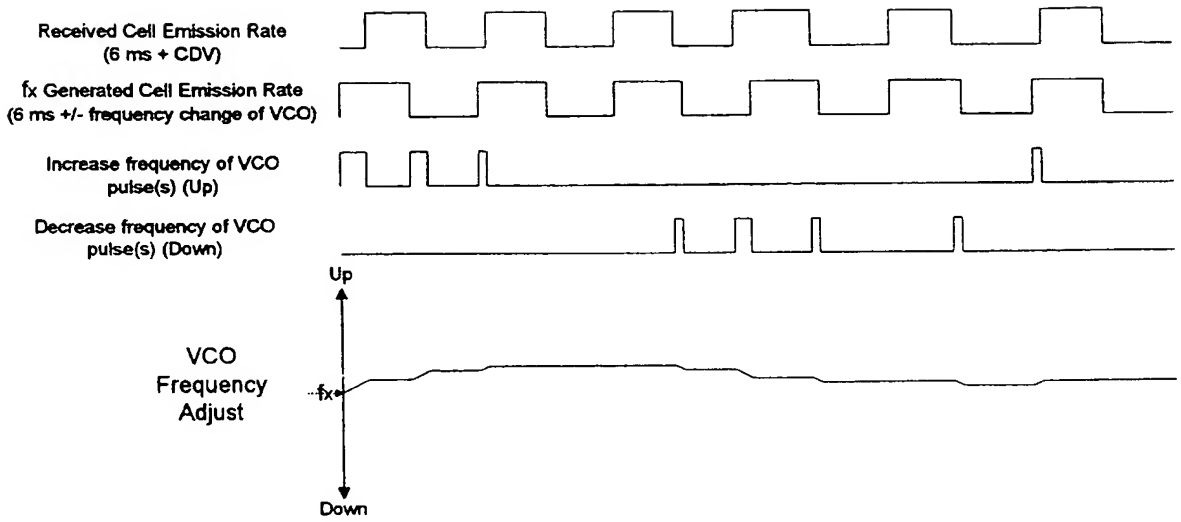
Received Cell Emission Rate
(6 ms + CDV)
fx Generated Cell Emission Rate
(6 ms +/- frequency change of VCO)
Increase frequency of VCO
pulse(s) (Up)
Decrease frequency of VCO
pulse(s) (Down)
Up
VCO
Frequency
Adjust
fx
Down

Fig. 5